ADVANCED SENSOR INTEGRATIONS

CLOCK GENERATOR PLL – AIP-PLL20M

FEATURES

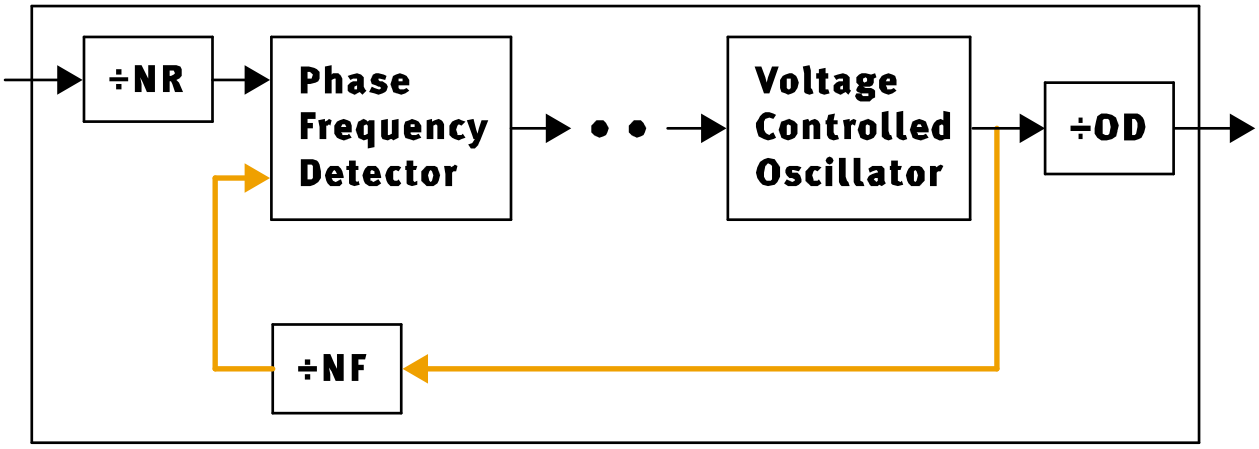
- Supply voltage: 3.3V
- Output frequency range: 32KHz - 1MHz
- Current consumption below 0.3mA
- Feedback divider values: 1 - 32
- Reference divider values: 1
- Period jitter: NDA required
- Output duty cycle: 50%
- Power-up/down control
- Power-down mode (consumption < 1uA)
- Total core area: NDA required
- Temperature: -40C to 125C
- Process technology: 0.35um digital CMOS

OVERVIEW

- Designed as a very flexible clock multiplier capable of muliplying an input clock from 1 to 32 with very low power consumption.
- Delivers optimal jitter performance over all multiplications settings.
- Ideal for implantable medical applications, portable devices and system clock generations.

IP STATUS

- **SILICON VERIFIED**



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